

NDS9407

60V P-Channel PowerTrench® MOSFET

General Description

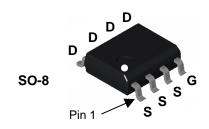
This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V-20V).

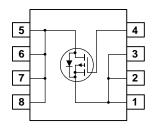
Applications

- · Power management
- Load switch
- · Battery protection

Features

- -3.0 A, -60 V. $R_{DS(ON)} = 150 \text{ m}\Omega$ @ $V_{GS} = -10 \text{ V}$ $R_{DS(ON)} = 240 \text{ m}\Omega$ @ $V_{GS} = -4.5 \text{ V}$
- · Low gate charge
- · Fast switching speed
- High performance trench technology for extremely low $R_{\mbox{\scriptsize DS(ON)}}$
- High power and current handling capability





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	
V_{DSS}	Drain-Source Voltage		-60	V
V _{GSS}	Gate-Source Voltage		±20	V
I _D	Drain Current - Continuous	(Note 1a)	-3.0	А
	- Pulsed		-12	
P _D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1.0	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +175	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
		(Note 1c)	125	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	

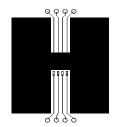
Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
NDS9407	NDS9407	13"	12mm	2500 units

Symbol	ctrical Characteristics T _A = 25°C unless otherwise noted			Tyro	Max	Units
Symbol	Parameter	Parameter Test Conditions		Тур	IVIAX	Ullits
Off Char	acteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{D} = -250 \mu\text{A}$	-60			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25°C		-45		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			−1 −10	μА
I _{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
I _{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-1	-1.6	-3	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25°C		4		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$V_{GS} = -10 \text{ V}, \qquad I_D = -3.0 \text{ A}$ $V_{GS} = -4.5 \text{ V}, \qquad I_D = -1.6 \text{ A}$ $V_{GS} = -10 \text{ V}, I_D = -3.0 \text{ A}, T_J = 125^{\circ}\text{C}$		78 99 122	150 240 250	mΩ
D(on)	On–State Drain Current	$V_{GS} = -10 \text{ V}, V_{DS} = -5 \text{ V}$	-12			Α
9rs	Forward Transconductance	$V_{DS} = -15 \text{ V}, I_{D} = -3.0 \text{ A}$		8		S
_	Characteristics	, ,				
C _{iss}	Input Capacitance	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V},$		732		pF
Coss	Output Capacitance	f = 1.0 MHz		86		pF
C _{rss}	Reverse Transfer Capacitance			38		pF
Switchir	ng Characteristics (Note 2)					•
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -30 \text{ V}, \qquad I_D = -1 \text{ A},$		8	16	ns
· ,	<u> </u>	$V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$		11	20	ns
t _r	Turn-On Rise Time	· ·		10	20	
	Turn–On Rise Time Turn–Off Delay Time				20	ns
t _{d(off)}		- -		10	20	ns
$t_{d(off)}$	Turn-Off Delay Time	I _F = -3.0 A,				_
d(off)	Turn-Off Delay Time Turn-Off Fall Time	$I_F = -3.0 \text{ A},$ $d_{iF}/d_t = 100 \text{ A/}\mu\text{s}$		10		ns
t _{d(off)} t t rr Q _{rr}	Turn-Off Delay Time Turn-Off Fall Time Diode Reverse Recovery Time			10		ns nS
t _{d(off)} t _f t _{rr} Q _{rr}	Turn-Off Delay Time Turn-Off Fall Time Diode Reverse Recovery Time Diode Reverse Recovery Charge	$d_{iF}/d_t = 100 \text{ A/}\mu\text{s}$		10 24 66	20	ns nS nC
id(off)	Turn-Off Delay Time Turn-Off Fall Time Diode Reverse Recovery Time Diode Reverse Recovery Charge Total Gate Charge	$d_{iF}/d_{t} = 100 \text{ A/}\mu\text{s}$ $V_{DS} = -30 \text{ V}, \qquad I_{D} = -3.0 \text{ A},$		10 24 66 16	20	ns nS nC nC
tr td(off) tt trr Qrr Qg Qgs Qgd	Turn-Off Delay Time Turn-Off Fall Time Diode Reverse Recovery Time Diode Reverse Recovery Charge Total Gate Charge Gate-Source Charge Gate-Drain Charge	$\begin{aligned} &d_{iF}/d_t = 100 \text{ A/}\mu\text{s} \\ &V_{DS} = -30 \text{ V}, &I_D = -3.0 \text{ A}, \\ &V_{GS} = -10 \text{ V} \end{aligned}$		10 24 66 16 2.2	20	ns nS nC nC
td(off) tf trr Qrr Qg Qgs Qgd	Turn-Off Delay Time Turn-Off Fall Time Diode Reverse Recovery Time Diode Reverse Recovery Charge Total Gate Charge Gate-Source Charge	$d_{iF}/d_t = 100 \text{ A/}\mu\text{s}$ $V_{DS} = -30 \text{ V}, \qquad I_D = -3.0 \text{ A},$ $V_{GS} = -10 \text{ V}$ and Maximum Ratings		10 24 66 16 2.2	20	ns nS nC nC

Notes:

 R_{8JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{8JC} is guaranteed by design while R_{8CA} is determined by the user's board design.



a) 50°C/W when mounted on a 1in² pad of 2 oz copper



b) 105°C/W when mounted on a .04 in² pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μ s, Duty Cycle < 2.0%

Typical Characteristics

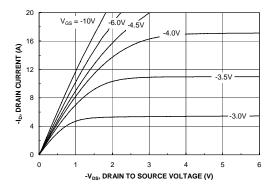


Figure 1. On-Region Characteristics.

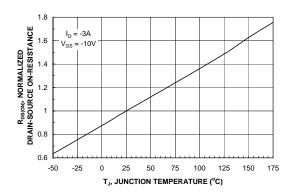


Figure 3. On-Resistance Variation with Temperature.

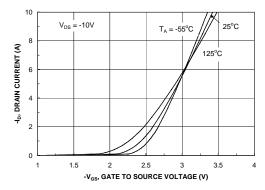


Figure 5. Transfer Characteristics.

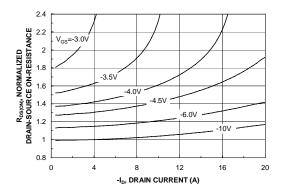


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

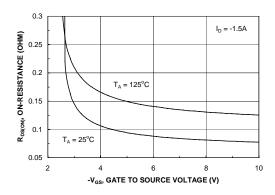


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

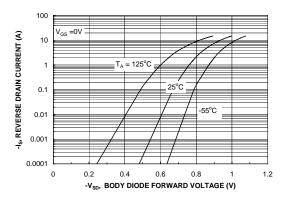
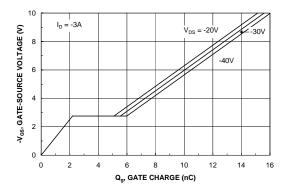


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



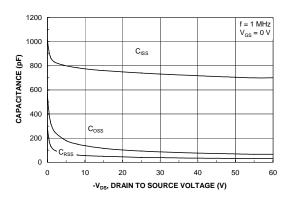
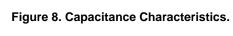
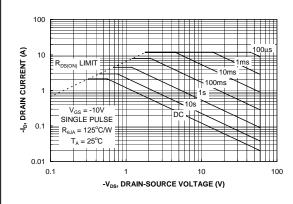


Figure 7. Gate Charge Characteristics.





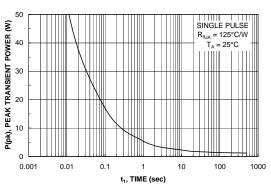


Figure 9. Maximum Safe Operating Area.



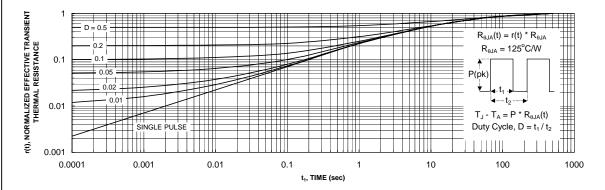


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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